We Claim:

1. An electrically operated memory element, comprising:

a substrate;

a pore of programmable resistance material formed above said substrate, said pore having a minimum lateral dimension less than 1300 Angstroms; and

a first dielectric layer formed between said pore and said substrate, at least a portion of said dielectric underlying at least a portion of said pore.

2. The memory element of claim 1, further comprising a spacer formed about a peripheral portion of said pore.

3. The memory element of claim 1, wherein said programmable resistance material comprises a phase change material.

4. The memory element of claim 1, wherein said programmable resistance material comprises a chalcogen.

5. An electrically operated memory element, comprising:

a substrate;

a pore of programmable resistance material formed above said substrate, said pore having a minimum lateral dimension less than a photolithographic limit; and

a first dielectric layer formed between said pore and said

substrate, at least a portion of said dielectric underlying at least a portion of said pore.

6. The memory element of claim 5, further comprising a spacer formed about a peripheral portion of said pore.

7. The memory element of claim 5, wherein said programmable resistance material comprises a phase change material.

8. The memory element of claim 5, wherein said programmable resistance material comprises a chalcogen element.

9. An electrically programmable memory element, comprising:

a first dielectric layer;

a first conductive layer formed over said first dielectric layer;

a second dielectric layer formed over said first conductive layer, said second dielectric layer having a pore therein, said pore having a minimum lateral dimension less that 1300 Angstroms;

a programmable resistance material disposed within said opening; and

a second conductive layer formed over said programmable resistance material.

10. The memory element of claim 9, further comprising:

a third conductive layer electrically coupled between said first conductive layer and a substrate, wherein substantially all electrical communication between said second conductive layer and said first conductive layer is through an edge portion of said second conductive layer.

11. The memory element of claim 10, wherein said third conductive layer comprises a sidewall layer.

12. The memory element of claim 10, wherein said third conductive layer is a conductive sidewall spacer or a conductive sidewall liner.

13. The memory element of claim 9, wherein said programmable resistance material comprises a phase change material.

14. The memory element of claim 9, wherein said programmable resistance material comprises a chalcogen element.

15. An electrically programmable memory element, comprising:

a first dielectric layer;

a first conductive layer formed over said first dielectric layer;

a second dielectric layer formed over said first conductive

layer, said second dielectric layer having a pore therein, said pore sized smaller that a photolithographic limit;

a programmable resistance material disposed within said pore; and

a second conductive layer formed over said programmable resistance material.

16. The memory element of claim 15, further comprising:

a third conductive layer electrically coupled between said first conductive layer and a substrate, wherein substantially all electrical communication between said second conductive layer and said first conductive layer is through an edge portion of said second conductive layer.

17. The memory element of claim 16, wherein said third conductive layer comprises a sidewall layer.

18. The memory element of claim 16, wherein said third conductive layer is a conductive sidewall spacer or a conductive sidewall liner.

19. The memory element of claim 15, wherein said programmable resistance material comprises a phase change material.

20. The memory element of claim 15, wherein said programmable

resistance material comprises a chalcogen element.

21. An electrically programmable memory element, comprising:

a first dielectric layer;

a first conductive layer formed over said first dielectric layer;

a second dielectric layer formed over said first conductive layer, said second dielectric layer having an opening therethrough to said first conductive layer;

a spacer disposed about a peripheral portion of said opening to form a pore;

a programmable resistance material disposed within said pore; and

a second conductive layer formed over said programmable resistance material.

22. The memory element of claim 21, wherein said spacer is formed by the method comprising the steps of:

forming a third dielectric layer over a peripheral portion of of said opening; and

removing a portion of said third dielectric layer.

23. The memory element of claim 21, further comprising:

a third conductive layer electrically coupled between said first conductive layer and a substrate, wherein substantially all

electrical communication between said second conductive layer and said first conductive layer is through an edge portion of said third conductive layer.

24. The memory element of claim 23, wherein said third conductive layer comprises a sidewall layer.

25. The memory element of claim 23, wherein said third conductive layer is a conductive sidewall spacer or a conductive sidewall liner.

26. The memory element of claim 21, wherein said programmable resistance material comprises a phase change material.

27. The memory element of claim 21, wherein said programmable resistance material comprises a chalcogen element.

28. An electrically operated memory element comprising:

a first conductive layer;

a first dielectric layer disposed over said first conductive layer, said first dielectric layer having an opening formed therein;

a dielectric spacer disposed about a peripheral portion of said opening to form a pore, said spacer formed by depositing a second dielectric layer over said opening and removing a portion

of said second dielectric layer;

a programmable resistance material disposed in said pore; and

a second conductive layer disposed over said programmable resistance material.

29. The memory element of claim 28, wherein removing said portion of said second dielectric layer comprises anisotropically etching said second dielectric layer.

30. The memory element of claim 28, further comprising:

a third conductive layer electrically coupled between said first conductive layer and a substrate, wherein substantially all electrical communication between said second conductive layer and said first conductive layer is through an edge portion of said second conductive layer.

31. The memory element of claim 30, wherein said third conductive layer comprises a sidewall layer.

32. The memory element of claim 30, wherein said third conductive layer is a conductive sidewall spacer or a conductive sidewall liner.

33. The memory element of claim 28, wherein said programmable resistance material comprises a phase change material.

34. The memory element of claim 28, wherein said programmable resistance material comprises a chalcogen element.

35. An electrically operated memory element, comprising:

a substrate;

a first dielectric layer formed over said substrate, said first dielectric layer having a sidewall surface formed therein;

a first conductive layer disposed on said sidewall surface;

a second dielectric layer disposed over said first conductive layer, wherein an edge portion of said first conductive layer is exposed on said sidewall surface;

a second conductive layer disposed over at least a portion of said exposed edge portion; and

a programmable resistance material electrically coupled to said second conductive layer.

36. The memory element of claim 35, further comprising a third dielectric layer formed over said second conductive layer, said third dielectric layer having an opening formed therethrough to said second conductive layer, said programmable resistance material deposited into said opening.

37. The memory element of claim 35, further comprising:

a third dielectric layer formed over said second conductive

layer, said third dielectric layer having an opening formed therethrough to said second conductive layer; and

a spacer formed about a peripheral portion of said opening to form a pore, said programmable resistance material disposed in said pore.

38. The memory element of claim 35, further comprising:

a third conductive layer formed over said second conductive layer;

a third dielectric layer formed over said third conductive, said third dielectric layer and said third conductive layer having an opening formed therethrough to said second conductive layer; and

a spacer formed about a peripheral portion of said opening to form a pore, said programmable resistance memory material disposed in said pore.

39. The memory element of claim 35, wherein the resistivity of said second conductive layer is greater than the resistivity of said first conductive layer.

40. The memory element of claim 38, wherein the resistivity of said second conductive layer is greater than the resistivity of said third conductive layer.

41. The memory element of claim 35, wherein said programmable resistance material comprises a phase change material.

42. The memory element of claim 35, wherein said programmable resistance material comprises a chalcogen element.

43. The memory element of claim 37, wherein said spacer comprises a dielectric material.

44. An electrically operated memory element, comprising:

a programmable resistance material; and

an electrode electrically coupled to said programmable resistance material, said electrode comprising a first conductive layer adjacent to said memory material and a second conductive layer remote to said memory material, said second conductive layer being edgewise adjacent to said first conductive layer.

45. The memory element of claim 44, wherein second conductive layer comprises a sidewall layer.

46. The memory element of claim 44, wherein said second conductive layer comprises a conductive sidewall spacer or a conductive sidewall liner.

47. The memory element of claim 44, wherein the resistivity of

said first conductive layer is greater than the resistivity of said second conductive layer.

48. The memory element of claim 44,. wherein said programmable resistance material comprises a phase change material.

49. The memory element of claim 44, wherein said programmable resistance material comprises a chalcogen.

50. A method of fabricating a pore, comprising:

providing a first material layer;

forming a second material layer over said first material layer;

forming an opening in said second material layer therethough to said first material layer;

disposing a third material layer over said opening; and

removing a portion of said third material layer.

51. The method of claim 50, wherein said removing said portion of said third material layer comprises anisotropically etching said third material layer.

52. The method of claim 50, wherein said first material layer comprises a conductive material.

53. The method of claim 50, wherein said second material layer comprises a dielectric material.

54. The method of claim 50, wherein said third material layer comprises a dielectric material.

55. A method of fabricating a programmable resistance memory element, comprising:

providing a first conductive layer;

forming a first dielectric layer over said first conductive layer;

forming an sidewall surface in said first dielectric layer;

forming a second dielectric layer onto said sidewall surface; and

removing a portion of said second dielectric layer to define a pore in said first dielectric layer;

forming a layer of programmable resistance material into said pore; and

forming a second conductive layer over said layer of programmable resistance material.

56. The method of claim 55, wherein forming a sidewall surface in said first dielectric layer comprises forming an opening an opening in said first dielectric layer therethough to said first conductive layer.

57. The method of claim 55, wherein said removing said portion of said second dielectric layer comprises anisotropically etching said second dielectric layer.

58. The method of claim 56, wherein forming said second dielectric layer comprises substantially conformally depositing said second dielectric layer into said opening.

59. The method of claim 55, wherein said removing said portion of said second dielectric layer comprises anisotropically etching said second dielectric layer.